(12) UK Patent Application (19) GB (11) 2 353 401 (13) A

(43) Date of A Publication 21.02.2001

(21) Application No 9927423.5

(22) Date of Filing 20.11.1999

(30) Priority Data
(31) 9919626 (32) 20.08.1999 (33) GB

(71) Applicant(s)
3Com Corporation
(Incorporated in USA - Delaware)
5400 Bayfront Plaza, Santa Clara,
California 95952-8145, United States of America

(72) Inventor(s)
Nigel Stuart Priest
William Thomas Phillips
Emsley Douglas Dacres
Graham Brian Hollands

(74) Agent and/or Address for Service
Bowles Horton
Felden House, Dower Mews, High Street,
BERKHAMSTED, Herts, HP4 2BL, United Kingdom

(51) INT CL[7]
G01R 31/312 31/316 , H01L 21/66

(52) UK CL (Edition S)
H1K KMA
G1U UR31312

(56) Documents Cited
EP 0805356 A2 EP 0277764 A2

(58) Field of Search
UK CL (Edition R) G1U UR31303 UR31312 UR31316 ,
H1K KMA
INT CL[7] G01R 31/303 31/312 31/316 , H01L 21/66
Online: WPI, JAPIO, EPODOC

(54) Abstract Title
An integrated circuit package incorporating a capacitive sensor probe

(57) A probe (18) for capacitative sensing is provided within a semiconductor package, thereby enhancing sensitivity and improving 'line of sight' for capacitative testing. The probe may be formed as part of a signal layer in a multi-layer package or as part of any layer that is electrically insulated from those elements to be tested by capacitative coupling.

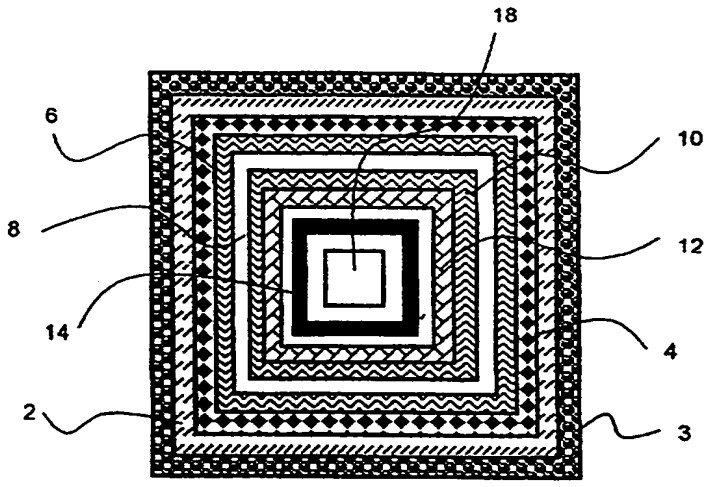

FIG.2

GB 2 353 401 A

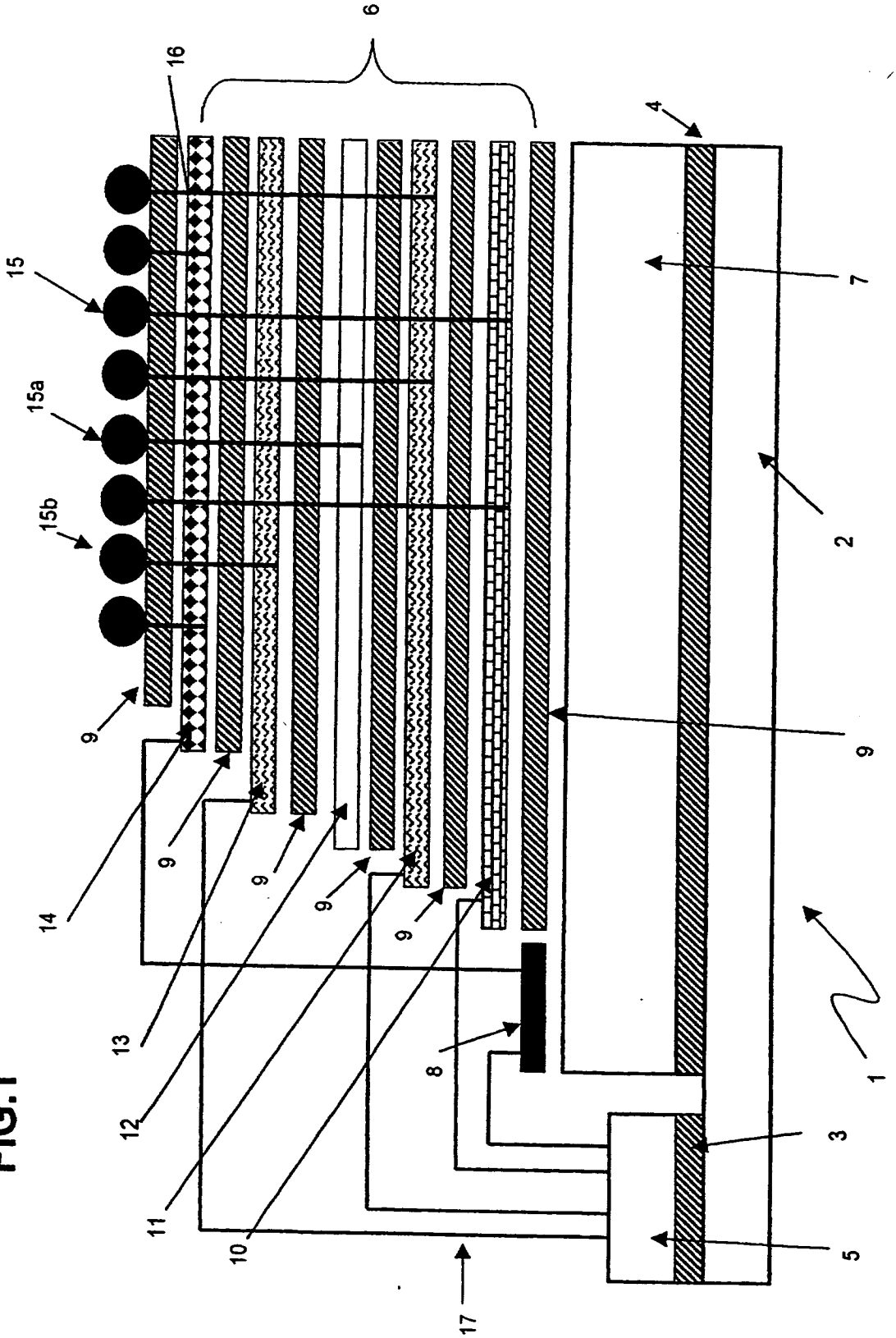

FIG.1

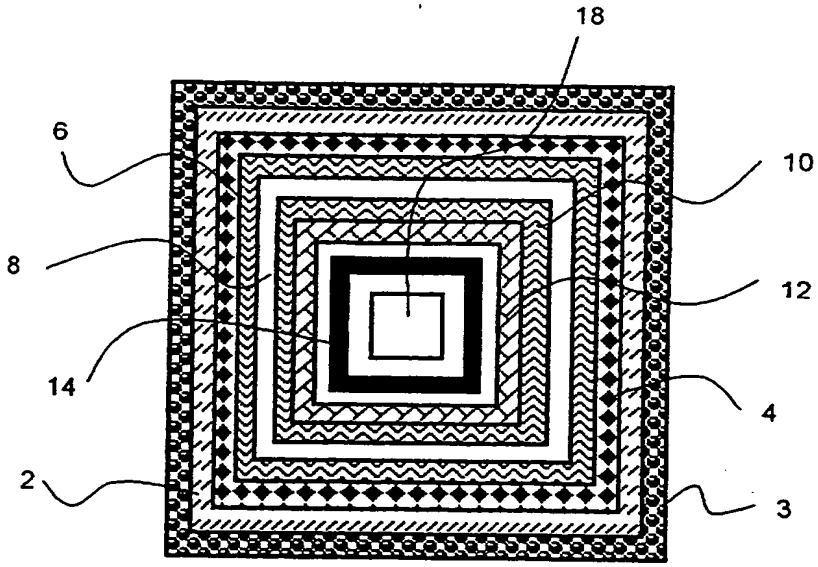

FIG.2

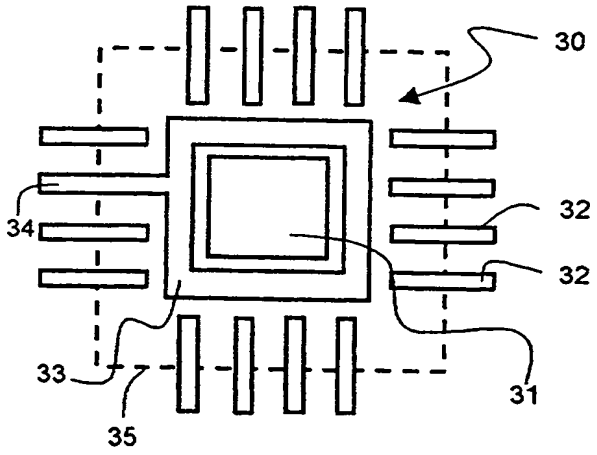

FIG.3

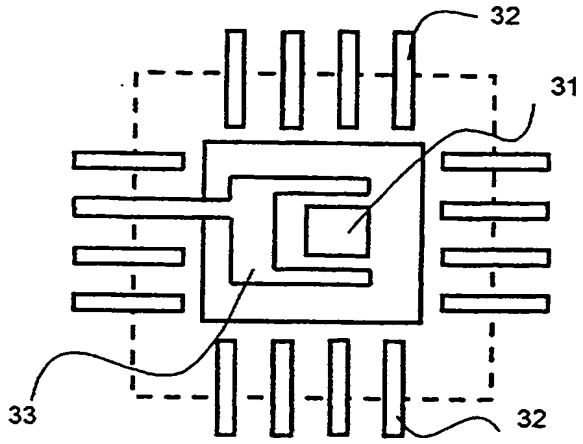

FIG.4

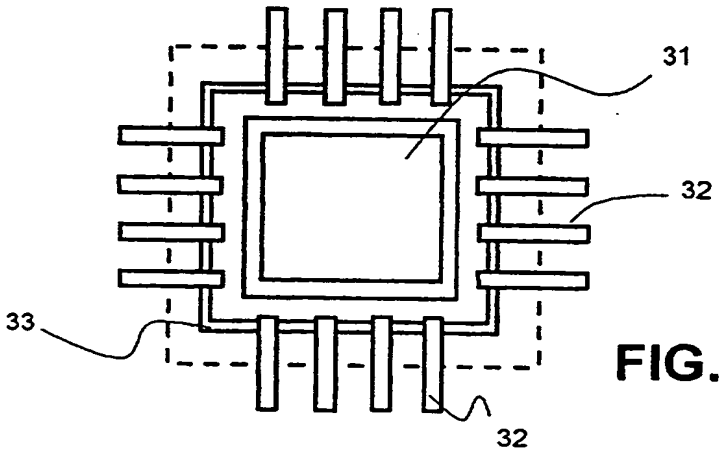

FIG.5

2353401

ELECTRONIC CIRCUIT INCLUDING CAPACITATIVE SENSING PROBE AND IMPROVED METHODS OF TESTING.

Field of the Invention

This invention relates to packages for semiconductor die elements and to electronic circuits. The invention has particular, but not exclusive, application to multi-layer electronic devices comprising at least one signal layer constituted by a printed or integrated circuit. Typically such devices include insulating layers, power layers and a heat sink or heat spreader. The present invention concerns an improved construction of such a multi-layer device to render it more easily testable, and the technique may also be applied more generally to other package types.

Background to the Invention

Fabrication of semiconductor components falls broadly into two stages. First is the fabrication of the semiconductor die and its associated metallisation. This is followed by mounting and electrical connection of the die to some kind of package that is suitable for handling and incorporation into larger circuit structures. Packages may include lead frames or other structures that have leads or terminals extending outwardly from the package. Other structures may have the outer terminals in the form of a grid of balls

Packages may include other elements of circuitry, for example as in a multi-layer electronic device package in which a semiconductor die is mounted alongside a multi-layer stack that includes printed or integrated circuit layers (often called 'signal' layers), a ground and/or power plane and a ball grid array. These various conductive layers are separated by insulating layers and the balls of the array interconnect by way of vertical traces extending through vias to the individual parts or layers to which they make predetermined contact.

Testing is a customary and important adjunct to the manufacturing and packaging process for electronic circuits. Different methods of testing have been devised and are in

use at the present time. One method, generally known as vector testing, requires the application of a large multiplicity of sets of binary signals (the vectors) to the input terminals of the circuit and the obtaining of the relevant sets of outputs. For circuits of any complexity, the vector testing mode is complex and often lengthy, and has the general disadvantage that the output vectors do not necessarily indicate directly the nature and location of a fault that causes them to depart from the vector values which would be produced if the circuit were operative in a fully correct manner.

Another known form of testing, described for example in United States patent US-5274336, is a capacitative method wherein a plurality of spring loaded conductive probes (known as a 'bed of nails') make selective ohmic contact directly with a device's input and output pins on one surface of a multi-layer device. A capacitative probe is constituted by an external plate, suspended over or otherwise separated from the circuit. The capacitance between a selected pin and the probe can be measured by stimulation from an AC source. Such a technique is useful for in circuit testing because if a terminal pin is not properly soldered to its trace on the printed circuit board, there is a reduction in capacitance in series with the capacitance formed with the capacitative probe. This change in capacitance may readily be detected and used to determine whether pins make proper connection (by means of adequate soldering) with the printed circuit, by for example discriminating between the actual measured capacitance and an expected or computed value.

One advantage of a capacitative sensing technique of this nature is that no knowledge of the core functionality of the device is required. The technique depends only on the physical properties of the packaging. It is simpler and in general much more rapid than 'vector' testing. Nevertheless, there are practical difficulties which render such a capacitative measuring technique potentially unsuitable. In particular, increasing miniaturization renders the technique less suitable, owing to the difficulty of determining the precise location of the fault. Furthermore, if the device includes a ground plane or for example a heat spreader which is not electrically isolated from other planes in the device, the obtaining of accurate results or occasionally any meaningful results from a capacitatively coupled test probe are difficult. This is particularly the case with multi-layer

structures having ball grid array external connection where 'line of sight' from the probe to the desired conductive element is more likely to be obscured by virtue of the vertical stacking arrangement. Thus despite its convenience and rapidity, capacitatively coupled probe testing appears to be unavailable for a variety of circuits owing to their construction.

Summary of the Invention

The present invention has as its main object a new construction for packages and circuits so as to make them better adapted for vectorless test techniques in general and capacitatively coupled testing in particular.

The invention is based on the location within a device package of a capacitative sensor probe such as a conductive sensing plane or plate which is not electrically utilised in the circuits of the device and is very preferably isolated conductively from any other plates, planes or circuits in the device. Such a probe can be disposed anywhere within the package, including as part of or adjacent any signal plane of the device and accordingly not be blocked by a ground or power plane or a heat spreader. The probe can be connected or tracked internally within the device to an externally accessible connection, such as a solder ball or lead, on an external face of the package in order to enable its connection to the circuit required for the application and sensing of a signal intended for measurement of capacitative values between the probe and other heads or terminals connected to the device. The probe may be a sensing plane that is part of a multi-layer stack, or be laterally displaced with respect to such a stack.

Brief Description of the Drawing

The invention is now described by way of example, with reference to the accompanying drawings in which:

Figure 1, illustrates in simplified form, and not to scale, a cross-section through a multi-layer electronic circuit device embodying the present invention;

Figure 2 is a schematic diagram of a plan layout of a device as shown in Figure 1;

Figure 3 is a schematic diagram of a lead frame incorporating a sensor probe;

Figure 4 is an alternative embodiment of lead frame package; and

Figure 5 is a further alternative lead frame embodiment.

Detailed Description of Preferred Embodiment

Figures 1 and 2 illustrate, by way of example, the general structure of a multi-layer electronic circuit package which is particularly adapted in accordance with the invention for capacitative testing. The invention is described in the context of this type of package as they exhibit particular testing problems. The package illustrated is an example only, the package shape, detail and layer construction may vary according to design requirements. Multi-die packages may also be constructed and the technique described can be applied in any situation or type of packaging with a variety of external connecting means such as balls, pins or leads.

The device 1 has an uppermost insulating layer 2 which is the support for a ball grid array 3 composed of a multiplicity of solder balls which are connected by 'vertical' traces, extending through vias in the relevant layers, to underlying layers of the device These traces should be without electrical contact to any conductive layer except with the respective layer to which they make predetermined connection Beneath the insulating layer 2 is a conductive ground layer or plane 4. Beneath this layer is a further insulating layer 5. The next underlying layer 6 is a 'signal' layer constituted by a printed or integrated circuit. The functionality of this circuit is of no particular importance to the invention.

Underlying the signal layer 6 is a further insulating layer 7. A conductive layer 8, hereinafter called 'sensing layer' is disposed below the insulating layer 7, the sensing layer 8 being thereby isolated conductively from the signal layer 6 but being capacitatively

coupled to it. Although there could be a respective sensing layer for each signal layer, in this example the sensing layer also serves for capacitative sensing of a second signal layer 10 which underlies the insulating layer 8 and is separated from it by an insulating layer 9. A yet further insulating layer 11 is disposed between the second signal layer 10 and a power layer 12 (which has a layout of the power rail VCC for the various circuits).

Beneath the power layer is another insulating layer 13 which is in this example substantially co-planer with a power ring 14. Layer 13 and ring 14 are disposed on a cavity layer 15 made for example of copper. This layer is separated by an insulating layer 16 from a conductive heat spreader 17.

Also on the heat spreader in this example is a semiconductor die 18, which is secured to the heat spreader by an adhesive layer 19, in this instance the heat spreader constituting a die attachment location or pad.

Conductive leads in the lead frame of the die are, in this example, connected, according to the requirements of the circuit device, to the power ring 14, the power layer 12 and the signal layers 6 and 10 by means of bond wires 20.

The foregoing is given by way of example only. It is not necessary that there be a multiplicity of signal layers. Moreover, the sense layer 8 need not be, as shown, in the middle of the layers making up the device but may, in general, be anywhere in the layers provided that, very preferably, it is adjacent, apart from separating insulation, to one or more of the signal layers. It follows that for complex devices having a multiplicity of signal layers there may be more than one sense layer such as the layer 8 or the sense layer may be part of a split layer, i.e. one having separate insulated sections on the same level. The power ring 14 could be split or reassigned to constitute a probe.

The layer 8 or each such layer is provided with external access by means of a wire or conductive trace which extends to at least one accessible terminal, herein constituted by one or more of the solder balls (3a) in the ball grid array (3).

It will be apparent that the sense layer 8 may be used for capacitative testing of, for example, the terminal connections such as the connection of solder ball 3b to signal layer 6, taking the place of the capacitative probe which is used in conjunction with the 'bed of nails' described in the aforementioned US patent. The usefulness of the known method is not thereby limited by the disposition of the ground plane or the heat spreader. However, the invention is not, obviously, limited to that method of testing.

Conventional features such as encapsulation have been omitted for the sake of brevity and simplicity.

In a modification, an amplifier which may be required for the performance of a capacitative test could be incorporated into the device (such as on die 18) to minimize the external components required for such a test.

It will be appreciated that the probe may be located in or on any part of the package where 'real estate' permits, which may include surfaces not normally utlilised and can vary depending upon the type of package. It is possible, as described later with reference to Figures 3 to 5, to include the probe as part of a lead frame, for example as a separate pad provided and supported similarly to a die attachment pad, or as a separate component such as an insulated supporting ring mounted beneath the lead ends. The important feature whatever the package type is that the signals or traces to be verified using capacitative sensing have a clear 'sight' of the probe without an intervening (conductive) ground or power plane or the like.

Figures 3 to 5 illustrate schematically how the invention may be applied in a simple lead frame package. In many instances lead frames are more complex and may include several attachment pads for multiple die assemblies or for use as heat sinks.

In Figure 3 a lead frame, illustrated generally by references 30 has a die attachment pad 31, a plurality of leads 32 and a capacitative sensor probe 33 surrounding the die attachment pad. As illustrated the capacitative sensor probe is shown directly connected in an integral manner with a lead part 34, but this is not essential, the probe could be wire

bonded to any lead. However, integral lead may enable utilisation as a heat sink. Dotted outline 35 shows the location of encapsulation that normally follows a wire bonding process.

Figure 4 is similar to Figure 3, but shows a different configuration for the probe. In this instance the probe does not completely surround the die attachment pad and has a form more similar to an adjacent pad. To maximise wire crossings, the probe extends around three sides of the die attachment pad.

Figure 5 illustrates a further alternative structure where the probe 33 is in the form of a ring beneath the leads 32. An insulating layer is disposed over the probe to prevent contact with the leads. As an alternative the probe could be positioned over the top of the leads and also optionally utilised as a spacer to inhibit wire sweep.

In the embodiments of Figures 3 and 4, and variations of that general type, the sensor probe may be part of a multi-layer structure on overlie such a structure.

Having described the incorporation of a probe into multi-layer and lead frame type packages, it will be appreciated that any package may be modified in this way or have its existing structures reassigned and suitably connected. As any fabrication stage has an attendant overhead, inclusion of the probe as part of other structures may be desirable. Apart from heat sinks and support structures other suitable parts that can be modified in this way include protective, shielding or anti-tamper layers.

Location of the probe within the package provides good capacitative linkage. Two factors which assist in this are the line of sight being unlikely to be completely obscured and the relatively close proximity of the probe to other parts of the package being tested. Typically when utilising the prior art external probes, capacitative measurements are of the general order, say, of around 20 to 200 femtofarads. In the present invention, when testing to a comparable conductive route, the reduced line of sight distance will render a large measurement raising the previous 20 femtofarads to 40 femtofarads, and putting within resolution linkages that previously were below a useful or measurable level. The value of

the capacitance measurement, compared with the expected value, can also be indicative of the nature and location of a fault.

A further modification of the technique described in detail in our copending application, is to incorporate the probe into the semiconductor die or its metallisation.

Claims

1. An integrated circuit package comprising:

a mounting for a semiconductor die;

a plurality of exposed terminal conductors (3);

a plurality of conductive linkages extending into the package from the exposed terminal conductors; and

a conductive, capacitative sensing probe disposed in the package and electrically connected to at least one (3a) of said terminal conductors, the sensing probe being capacitatively related to at least some of the conductive linkages.

2. An integrated circuit package according to claim 1 in which the conductive linkages include a multiplicity of stacked conductive layers (4, 6, 8, 10, 12) including at least one signal layer (6) and the sensing probe is capacitatively coupled to the signal layer.

3. An integrated circuit package according to claim 2 in which the sensing probe is a conductive layer (8) disposed as one of the stacked conductive layers.

4. An integrated circuit package according to claim 2 in which the sensing probe is a conductive layer disposed laterally adjacent the stacked conductive layers.

5. An integrated circuit package according to claim 1 in which the probe forms part of a lead frame assembly.

6. An integrated circuit package according to claim 1 in which the probe is formed as a ring.

7. An integrated circuit package according to claim 6 in which the probe is disposed adjacent the die mounting area.

8. An integrated circuit package according to claim 1 in which the probe forms part of a die mounting assembly.

9. An integrated circuit package in which the probe is disposed such that bonding wires connecting a die to the conductive linkages pass over at least a part of the probe.

10. An integrated circuit package in which the probe also comprises a protective or tamper resistant structure.

11. An integrated circuit comprising:

a semiconductor die;

a package for the semiconductor die;

a plurality of exposed terminal conductors (3);

a plurality of conductive linkages extending into the package and to the die from the exposed terminal conductors; and

a conductive capacitative sensing probe disposed in the package and electrically connected to at least one (3a) of the terminal conductors, the sensing probe being capacitatively related to at least some of the conductive linkages.

12. An integrated circuit according to claim 11 in which the probe is part of the package.

13. An integrated circuit according to claim 11 in which the probe is part of the die.

The Patent Office

INVESTOR IN PEOPLE

Application No: GB 9927423.5
Claims searched: 1-13

Examiner: SJ Morgan
Date of search: 17 February 2000

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.R): H1K(KMA); G1U(UR31312,UR31303,UR31316)

Int Cl (Ed.7): H01L 21/66; G01R 31/303, 31/312, 31/316

Other: Online: WPI, JAPIO, EPODOC

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	EP 0 805 356 A2	(HEWLETT-PACKARD) See line 40, column 8 - line 31, column 12	1, 6-8, & 11-13
X	EP 0 277 764 A2	(WESTINGHOUSE) See line 28, column 4 - line 16, column 5	1, 7, 8, 11, & 12

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.